On Board Computers

December 2017

Avionics

- *The Avionics Embedded System (AES) includes the hardware (processor, communication buses, equipments, instruments) and software required for the command & control of the spacecraft, its telecommand and telemetry handling, its failure detection, isolation and recovery and all the mission and vehicle management functions including all functional chains.*

  The AES is the brain of the spacecraft and therefore is a vital organ for the execution of onboard functions.

  It represents today between 30 and 70 % of the platform non-recurrent development costs (50% in average for an ESA mission).

On Board Computer

GAÏA

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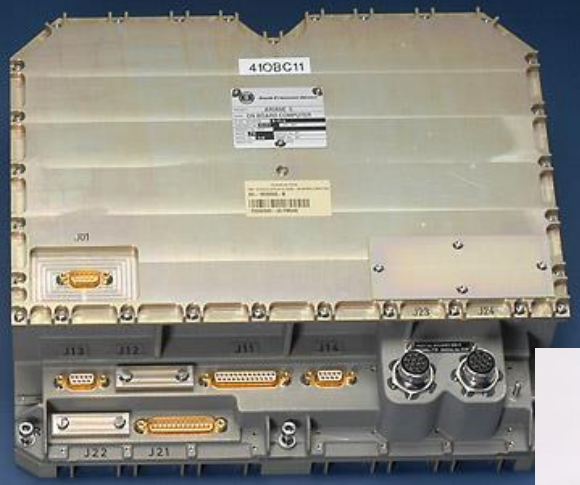


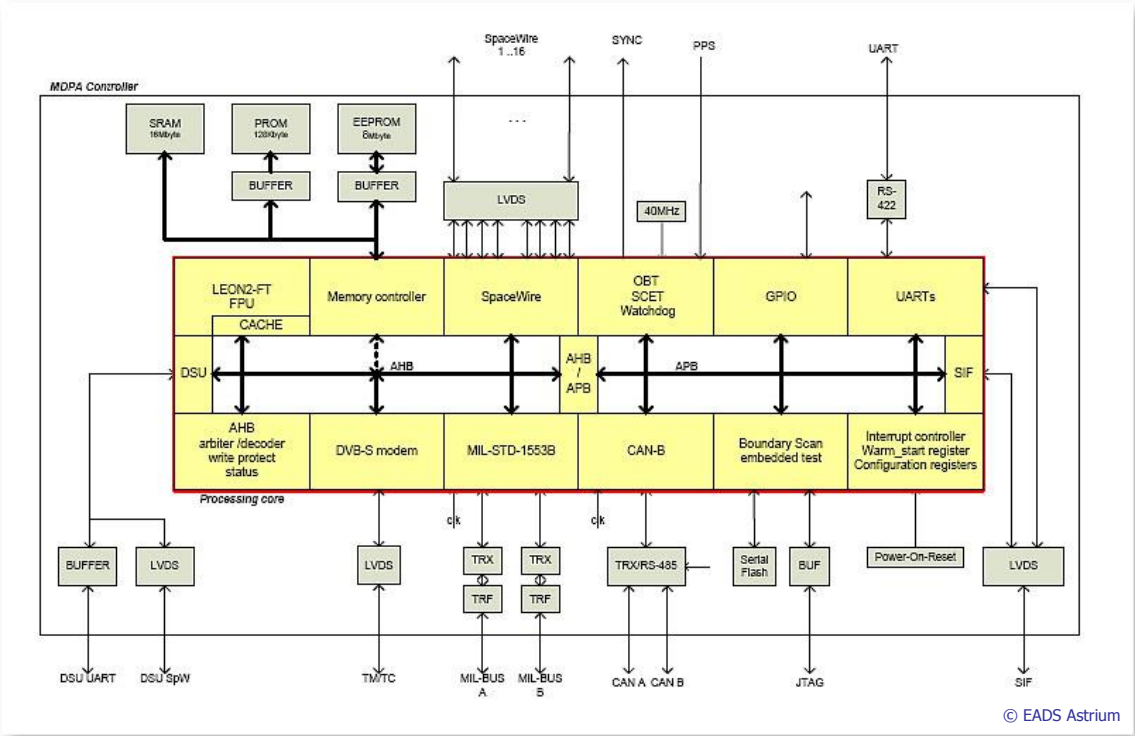
VEGA

GALILEO IOV OBC

Payload Data Handling Unit

PDHU

© EADS Astrium



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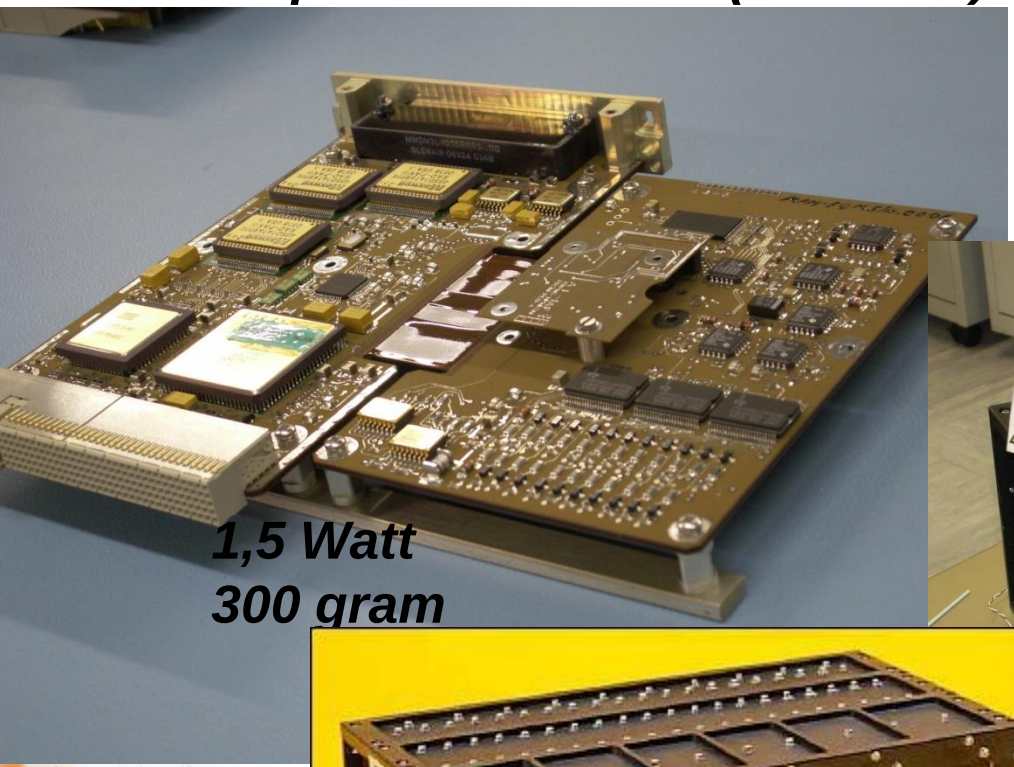
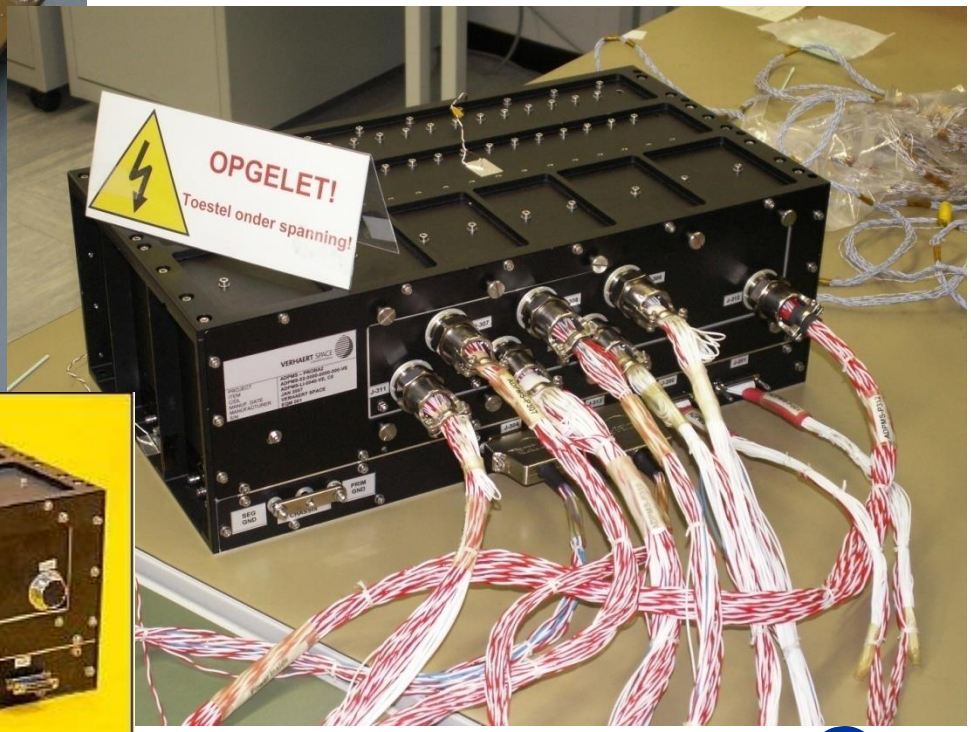
Advanced Data & Power Mgt System

The LEON processor board (unfolded)



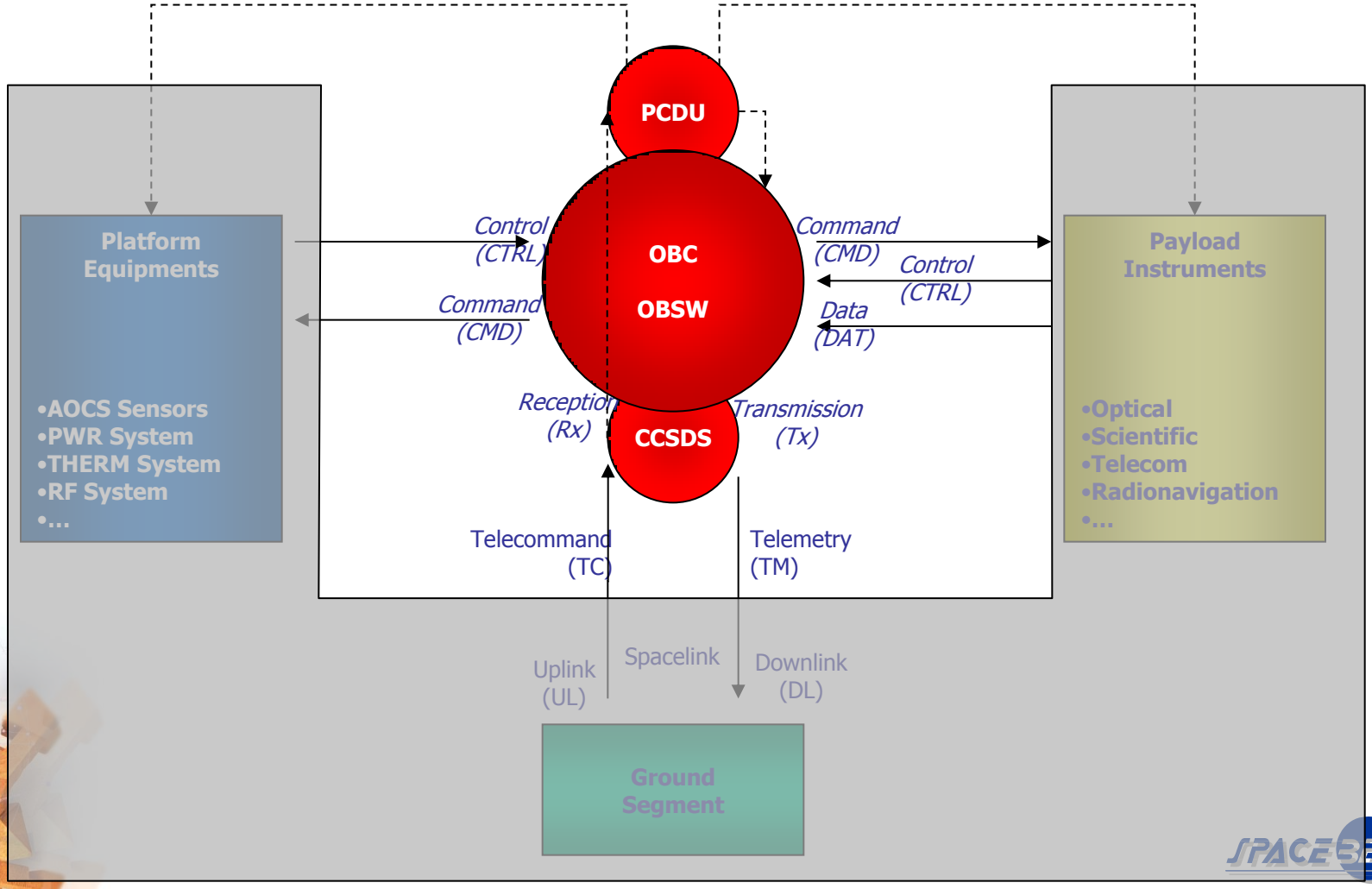
1,5 Watt
300 gram

ADPMS under test

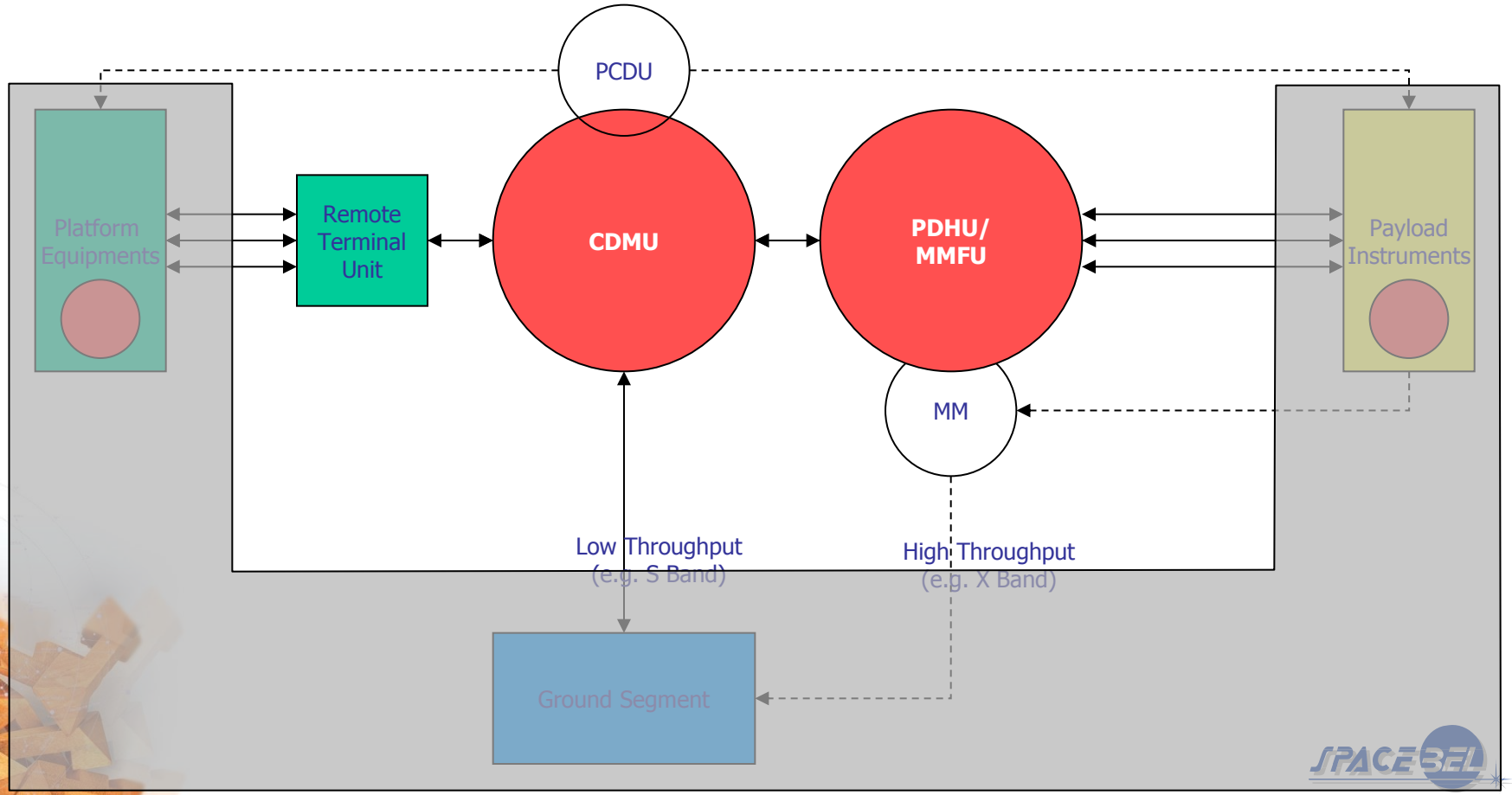


Avionics

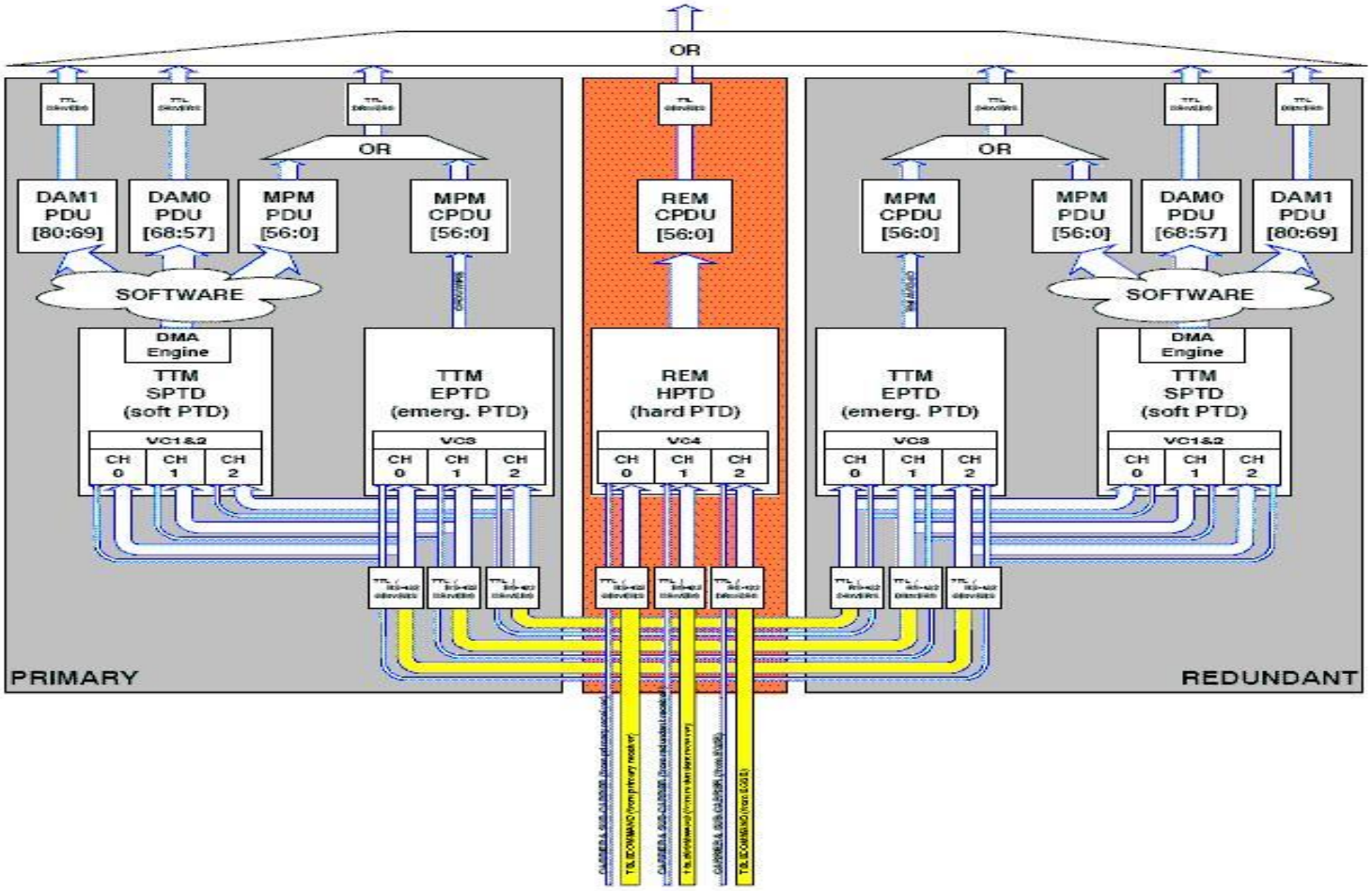
Avionics: Overview



Avionics: Overview (cont.)

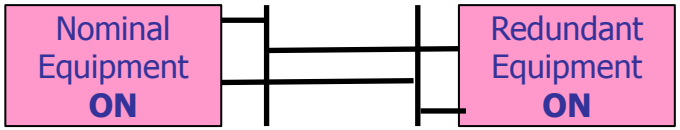


Avionics: Redundancy



Avionics: Redundancy

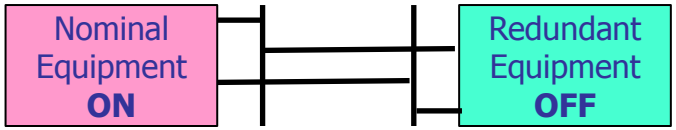
Hot Redundancy



Both nominal and redundant equipment are On and running in parallel

Mandatory if no way to select redundant equipment
Advantage: no service interruption
Drawback: reliability, consumption

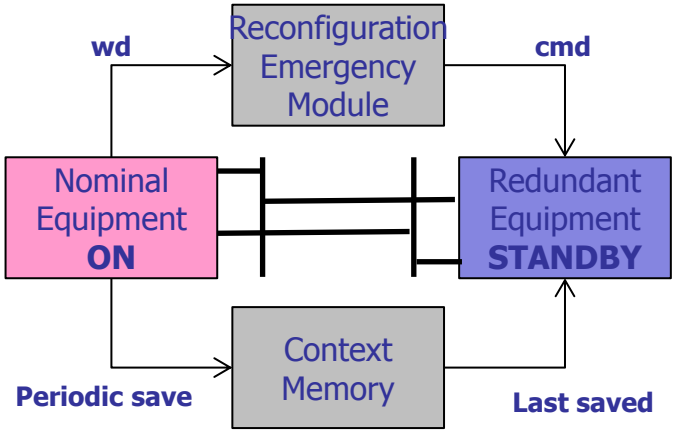
Cold Redundancy



Nominal equipment is On and running while Redundant equipment if Off and not running

Advantage: higher reliability
Drawback: failover time

Lukewarm Redundancy



Nominal equipment is On and running while Redundant equipment if On but Halted and not running

Typical of On Board Computer

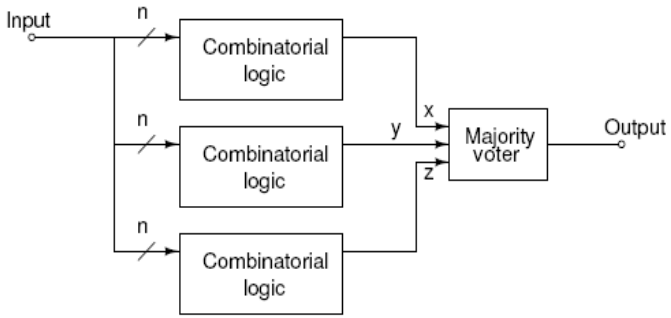
Avionics: Hostile Environment

- **Temperature**: extreme conditions
  - Temperature range solar cells -150 → +100 °C
  - Packaging, isolation and heaters: reduction to -20 → +50 °C
  - Commercial electronics don't fit the bill : 0 → 70 °C
    (mil range -55 → +125 °C)

- **Ion radiation** : electron, proton, heavy ion (solar flare, van Allen belts)
  - Cumulated Effect:
    - Modification of the component characteristics
  - Single Event Effects:
    - SET: Single Event Transient (glitches) non destructive
    - SEU: Single Event Upset (swap) non destructive
    - SEL: Single Event Latchup (CMOS)
    - SEB: Single Event Burnout (MOSFET) destructive
    - SEGR: Single Event Gate Rupture destructive

Avionics: Protection Means

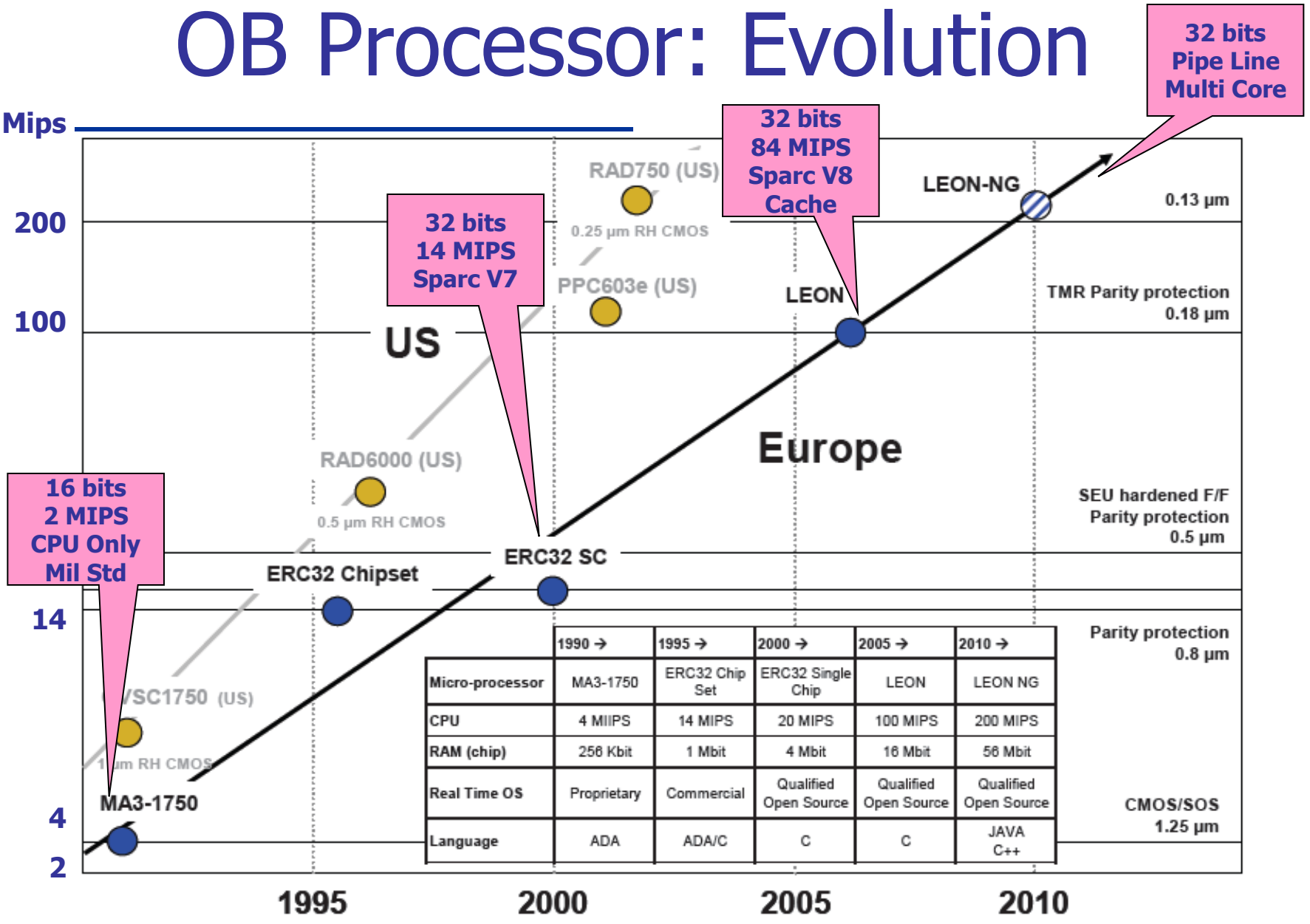
- **Radiation Protections**
  - Shielding
  - Box design
  - Positioning in the S/C
  - Technology choices
  - Build in electronic protection



- **Fault Tolerance**
  - Ability to support temporary or definitive modification or suppression of functionality
  - Redondancy
    - Processing: Spatial or Temporal Redundancy and Majority Voting
    - Duplicate the system: when a system is faulty, switch on the other one
    - Permit to eliminate the faulty system from the decision path (TMR technology)
    - Data Redundancy through coding, (RS, CRC, etc)
      - Error Detection and Correction (EDAC) on memory
      - Memory scrubbing to "clean" changed memory

ON BOARD PROCESSORS

OB Processor: Evolution



	1990 →	1995 →	2000 →	2005 →	2010 →
Micro-processor	MA3-1750	ERC32 Chip Set	ERC32 Single Chip	LEON	LEON NG
CPU	4 MIPS	14 MIPS	20 MIPS	100 MIPS	200 MIPS
RAM (chip)	256 Kbit	1 Mbit	4 Mbit	16 Mbit	56 Mbit
Real Time OS	Proprietary	Commercial	Qualified Open Source	Qualified Open Source	Qualified Open Source
Language	ADA	ADA/C	C	C	JAVA C++

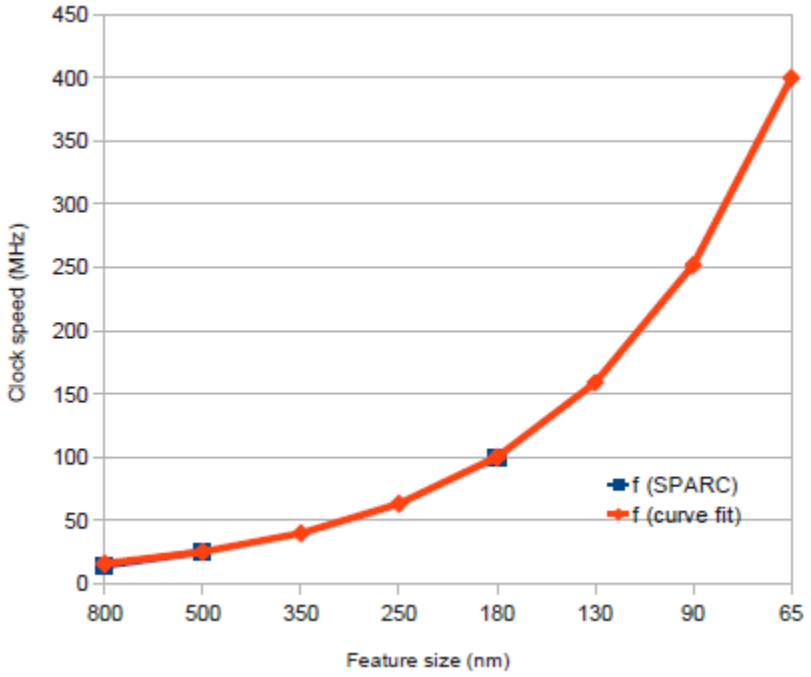
OB Processor: Frequency Increase

Increase of the processor clock frequency is a method of achieving higher performance. This however leads to increase of processor power dissipation figure.

Clock Speed of SPARC Architectures*

mid 90's	end 90's	mid 00's
ERC32 3-Chip Set	ERC32 Single Chip	LEON2-FT AT697
ATMEL (TEMIC)	ATMEL (TEMIC)	ATMEL
0.8 mm	0.5 mm	0.18 mm
SPARC V7	SPARC V7	SPARC V8
10 MIPS 14 MHz	20 MIPS 25 MHz	85 MIPS 100 MHz

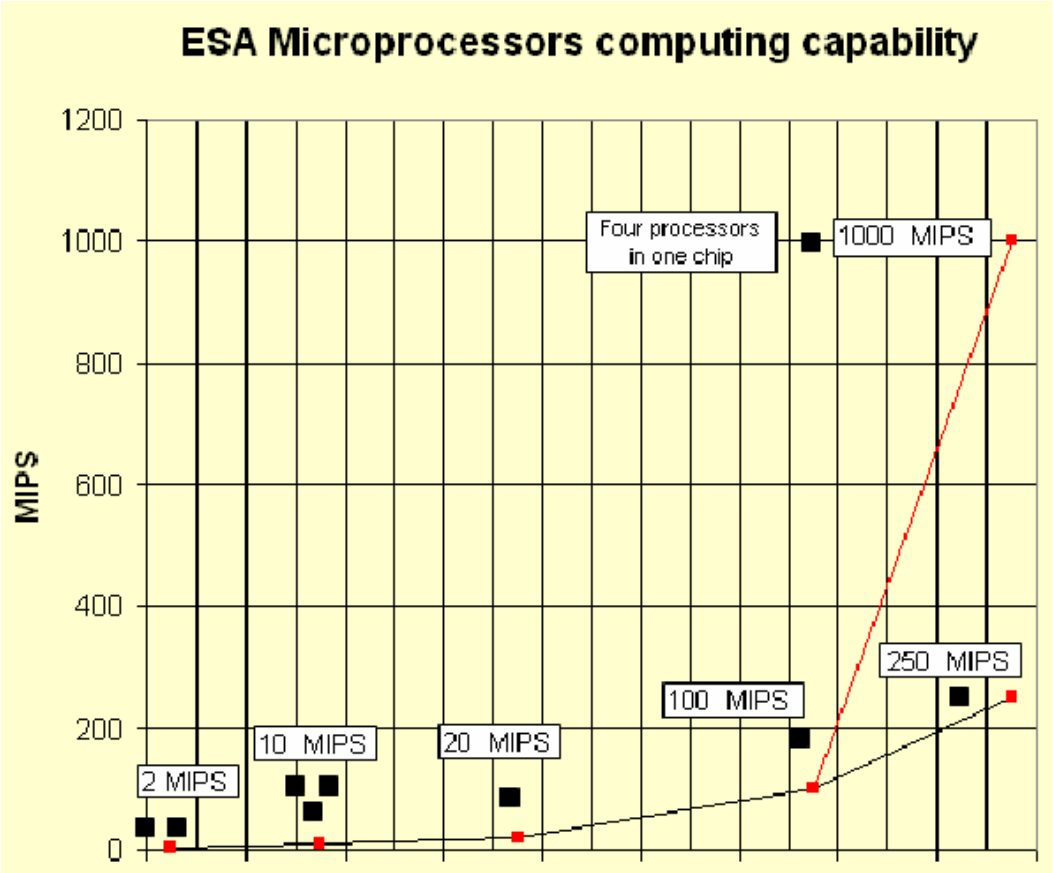
Extrapolating to 90 / 65 nm we obtain 250 / 400 MHz



OBP: Multi Core

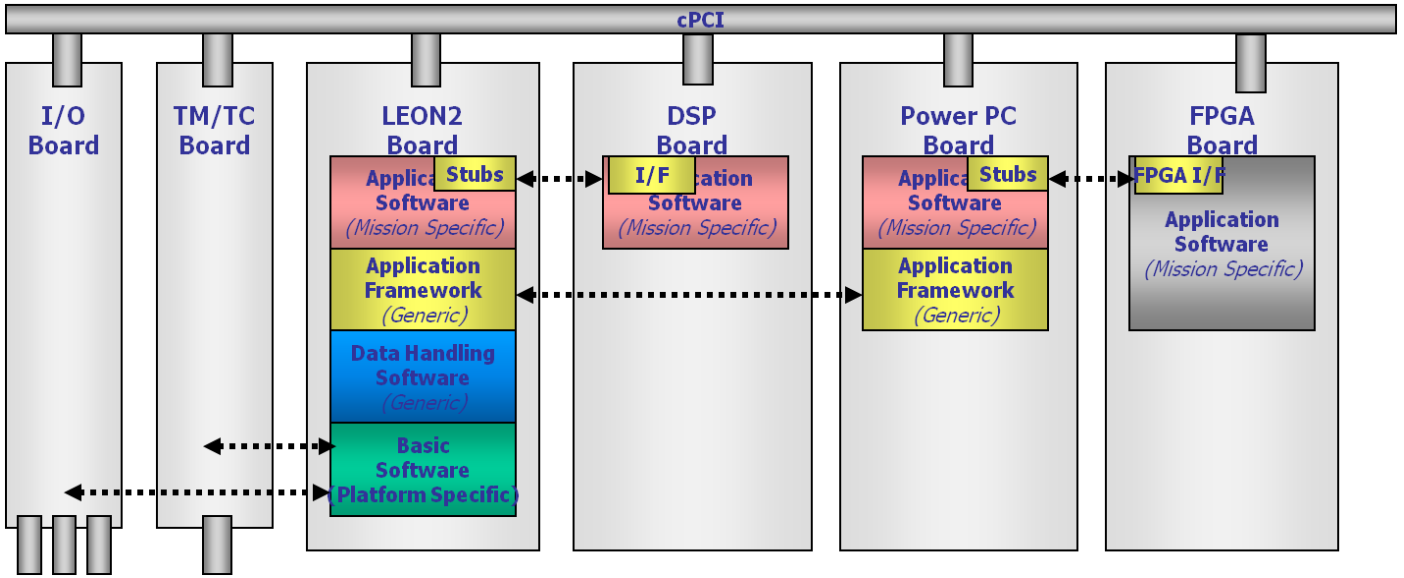
Multi-core architecture is an alternative architectural solution that has the main advantage to increase the platform performance without increasing the power consumption

	frequency	power dissipation increase	perfomance increase	remark
	1%	3%	0.60%	from Intel Corp. for <100nm (http://bcove.me/robm4kag)
example 1	15%	45%	9%	monocore
example 2	30%	90%	18%	monocore
example 3	-15%	~	180% Amdahl's Law $S_N = \frac{1}{(1-P)+\frac{P}{N}}$	Dual core

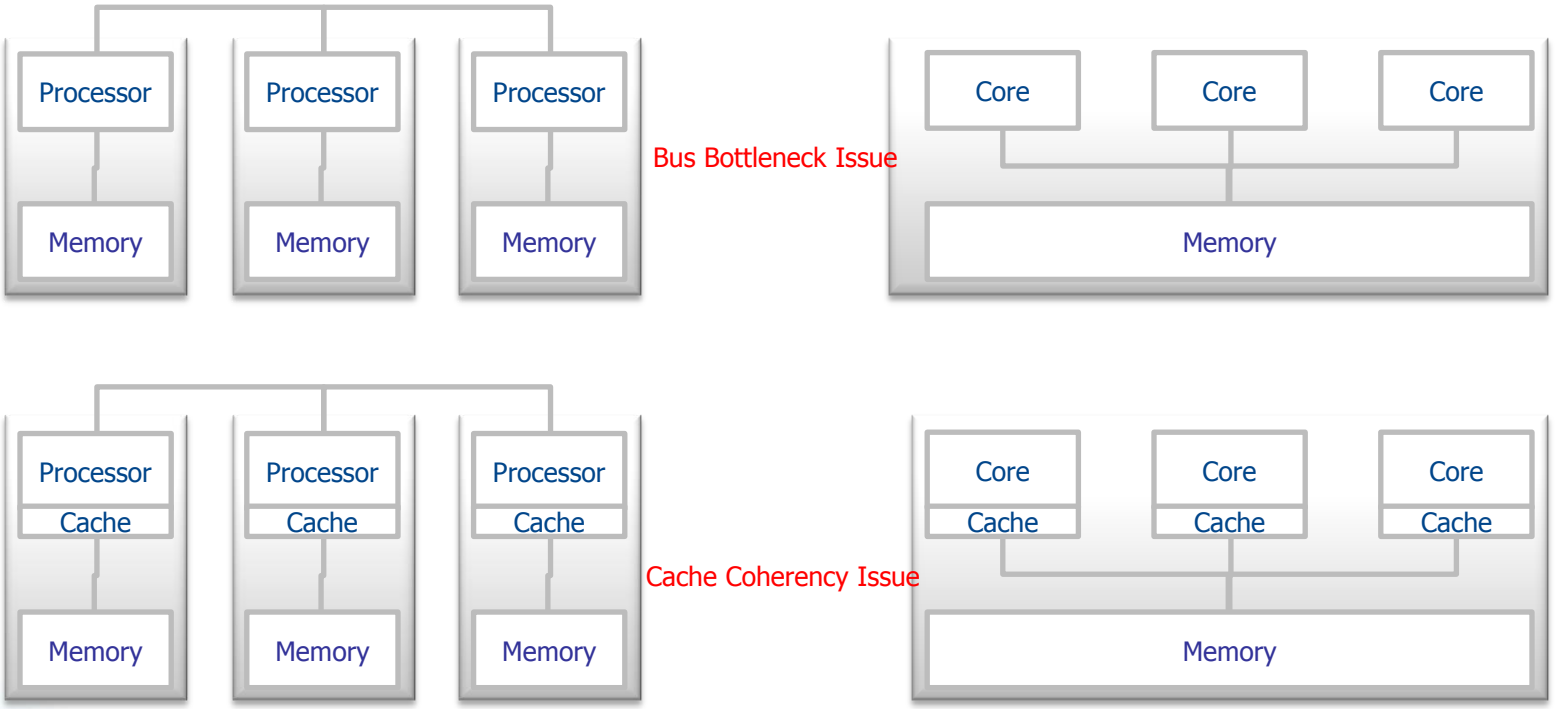


OBP: Multi Processor

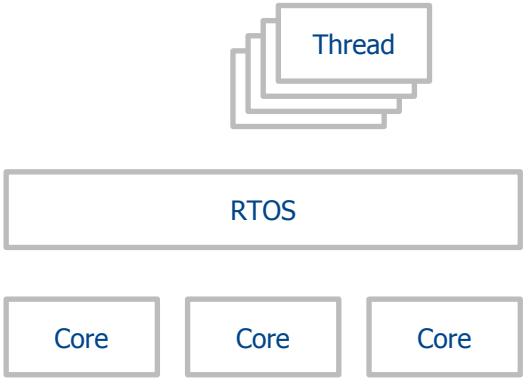
Multi-processor architecture is yet another alternative architectural solution that allows for distributing the processing (e.g. image processing, complex gnc algorithms), on specialized, dedicated hardware (e.g. µp, dsp, fpga)



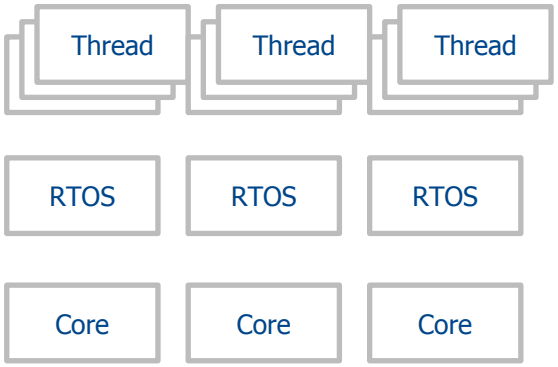
Processors vs Cores



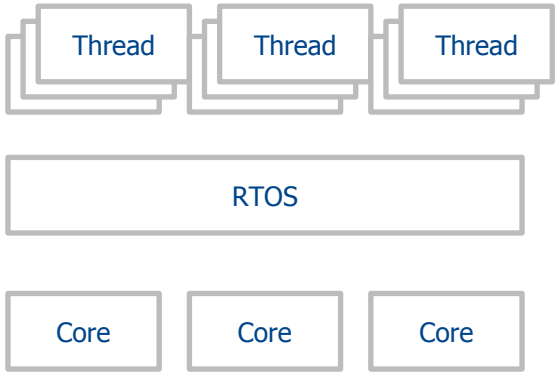
SMP vs AMP



Symmetric Multi Processing



Asymmetric Multi Processing



Supervised Asymmetric Multi Processing

OB MEMORY

On Board Computer Memory

- Memory types
  - **PROM** (Programmable Read Only Memory)
    16 – 256 KB
    Board boot and init SW
  - **EEPROM** (Electrically Erasable Programmable Read Only Memory)
    2 – 8 MB
    the mission SW boot container, also used for safeguard
  - **SRAM** (Static Random Access Memory)
    4 – 16 MB;
    the workplace that contains executing SW and variables
  - **SDRAM** (Synchronous Dynamic Random Access Memory)
    16 to 512 MB
    slower RAM typically used for mass storage

SRAM: data bit is stored in the state of a flip-flop (transistor logic - No power for Data Retention)

DRAM: data bit is stored in the electric charge of a nano capacitor (Frequent Refresh Cycles, Volatile)

MRAM: Magnetoresistive Random Access Memory (non-volatile magnetic storage)

ROM: uses a metal mask to permanently enable/disable selected transistors instead of storing a charge in them

FLASH: a kind of EEPROM erased and written in large blocks, read in a random access fashion (Non Volatile)

SDRAM, DDR SDRAM, FeRAM, MRAM, CRAM, PRAM

On Board Data Storage

- **Playing Tapes Storage** (Till 2000)
  - Mass Memory based on back and forward magnetic tapes.
  - Record in forward and play back in reverse (no time to rewind)
  - Robust to power failures

- **Solid State Mass Memory** (Nowadays)
  - Processor board can have 512 MB SDRAM Mass memory
  - Extra board could hold a GB (with battery back-up)
  - Very big Mass Memory units with almost unlimited size can be made in a very compact way (SDRAM or flash EPROM)
    - Interface through fast serial links (E.g. SpaceWire)
    - Mostly used for high resolution image satellites (e.g. 12 TB at EOL for Sentinel 2)

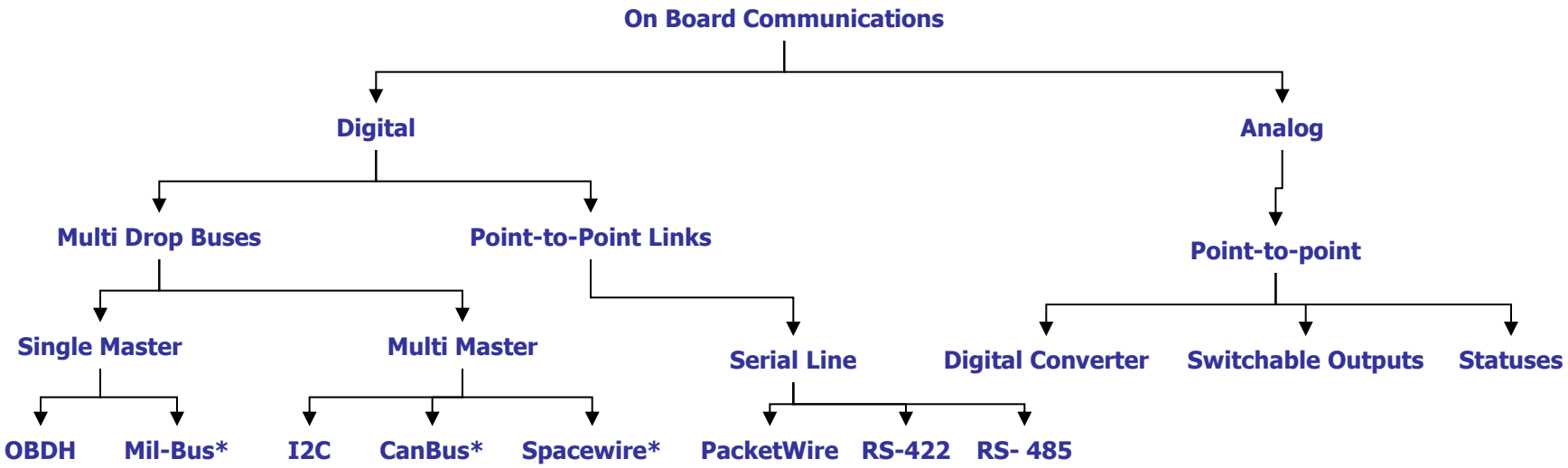
Storage Capacity, Transfer Data Rate,
Power for Data Retention, Power for Data Access,
Write Endurance, Sensitivity to Single Event Effects
High Speed Error Detection, High Speed Error Correction,
File Management System, Hardware Software Partitioning, Simultaneous Accesses

OB COMMUNICATIONS

On Board Communications Budget

Flow (Proba 2)	From -> To	Mbps
TC segments	Ground → Spacecraft	2
TM/TC CLCW protocol feedback	TC/TM channels	0,01
TM Packets	TM → ground	2 x 66
AOCS control	OBSW → Eqts	0,1
AOCS telemetry	Eqts → OBSW	0,1
Payload control	OBSW → Payload	0,1
Payload Telemetry	Payload → OBSW	0,01
Spacecraft SW housekeeping	Eqts → OBSW	0,01
REM context writing	OBSW → REM	0,01
REM Watchdog kicking	REM → OBSW	0,01
PCM/PDM control	OBSW → PCM/PDM	0,01
PCM/PDM Telemetry	PCM/PDM → OBSW	0,01
Spacecraft HW housekeeping	Eqts → OBSW	0,01
REM housekeeping	REM (TM) → ground	0,01
Payload Data TM packets	Payload → TM	20

On Board Communication



Trade offs to be made:

- Power consumption
- Silicon surface, board surface
- Connectors and wiring harness (6 to 10 % of weight of a satellite)
- Performance (throughput, response time)
- Isolation and fault propagation
- Intelligence required at slave end
- Required processing overhead

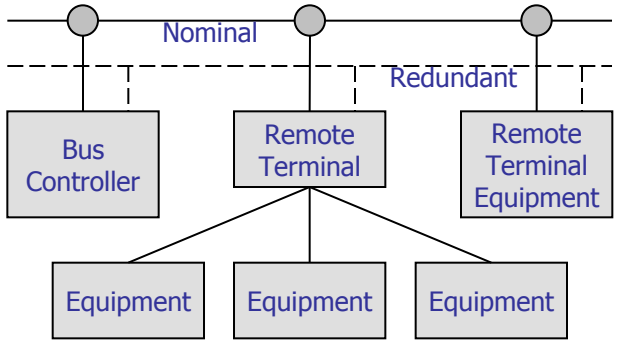
*may be redundant

Total harness weight (cables and connectors) may reach 6 to 10% of total satellite mass

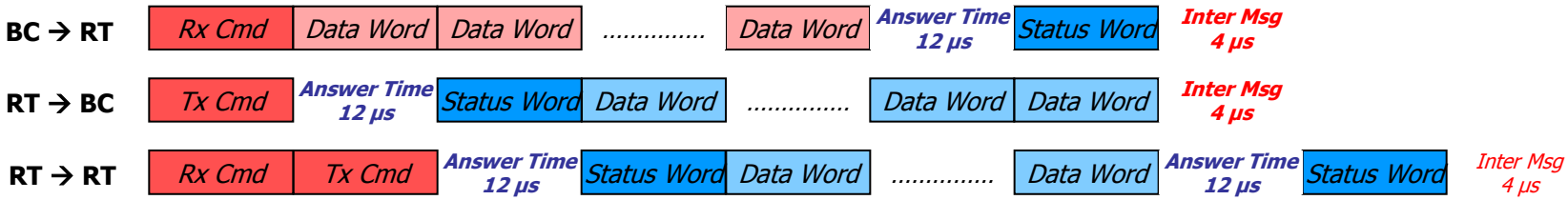
On going studies investigate on board wireless communications

MilBus Basics

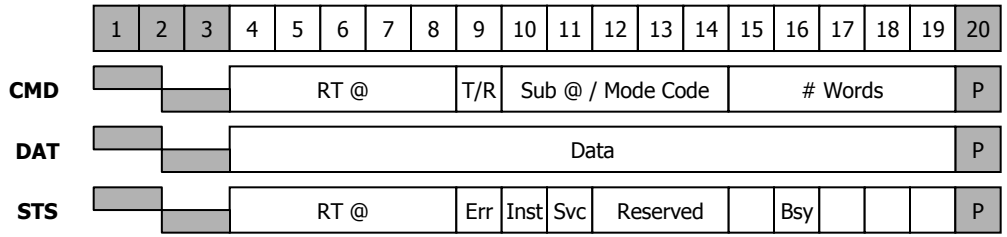
- From aircraft industry
- Mil-Std-1553-B Standard
- Multi Drop Bus
- Master/Slave
- Single cable
- Half Duplex
- Asynchronous
- Redundant (cross strapping)
- 1 Mbps (650 Kbps effective)
- Manchester Bi Phase Coding



1 Msg = 1 to 32 Words



1 Word = 16 Bits



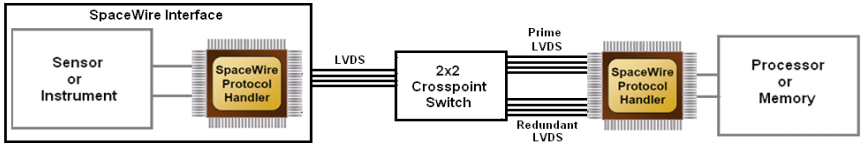
Spacewire Basics

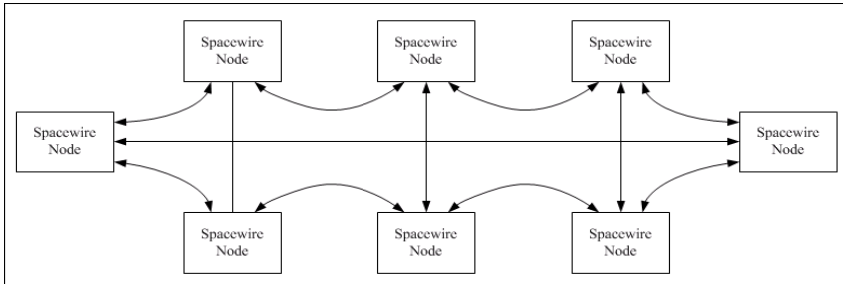
- High Speed Serial Link
- Fairly Simple
- High data rate (up to 400 Mbps)
- Low power consumption

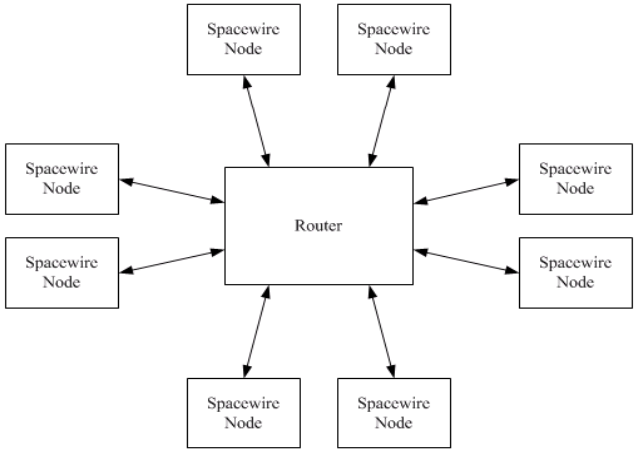
- Promoted by ESA, based on IEEE 1533, DS Link, Transputer Technology
- Physical interface requires LVDS-tranceivers

- Packet based <Destination Address><Cargo><End_of_Packet>

- SpaceWire **Router** connects a number of SpaceWire link interfaces (receiver to transmitter ports)
- Group Adaptive Routing: group of links may be configure to increase throughput (bandwidth sharing) or fault tolerance
- Allow for different topologies following use needs







CAN Bus Basic

- Controller Area Network (CAN)
  - Automotive
  - Bosch / Intel

Ethernet Basics

- Deterministic Ethernet
  - AFDX
    (Avionics Full Duplex Switched Ethernet)
  - TT Ethernet
    (Time Trigered Ethernet)

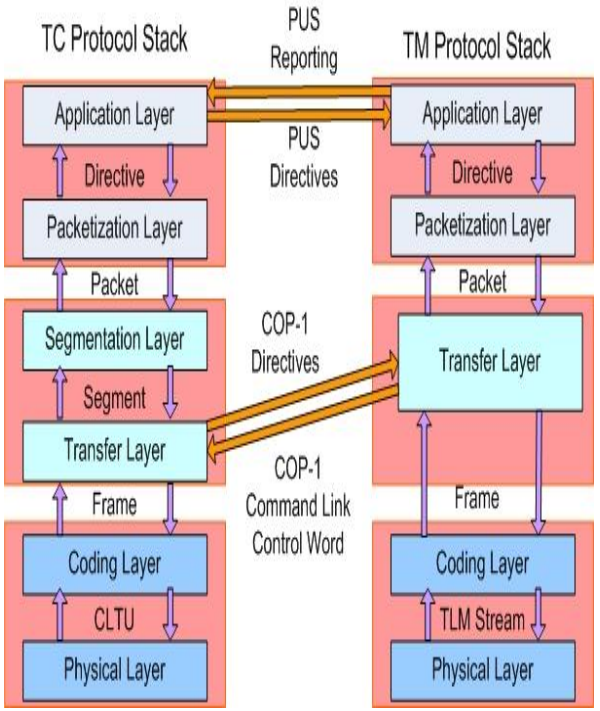
Space Link Basic

- Radio Frequency
  - L-Band, S-Band, X-Band (Science Data)
  - Delay and Disruption Tolerant
  - Tracking and Ranging
  - Telecommand Uplink
  - Telemetry Downlink

GND COMMUNICATION

TC Telecommands

- Receives TC bitstream from antenna/receiver
  - Hardware decoding of TC data streams:
    - Decoding bitstreams, error detection and correction, de-randomisation, overrun detection
    - Isolation of CLTU Command link Transmission Unit (which can contain several TC's)
    - Generate FAR Frame Analysis Report for CLCW, send to TM module (COP-1 protocol)
    - Sends emergency TC's directly to associated pulse generators
  - Sending of TC's to SW decoder
- Pulse generation (Pulse Distribution Unit)
  - Generates and distributes pulses without software intervention (reliability, precision)



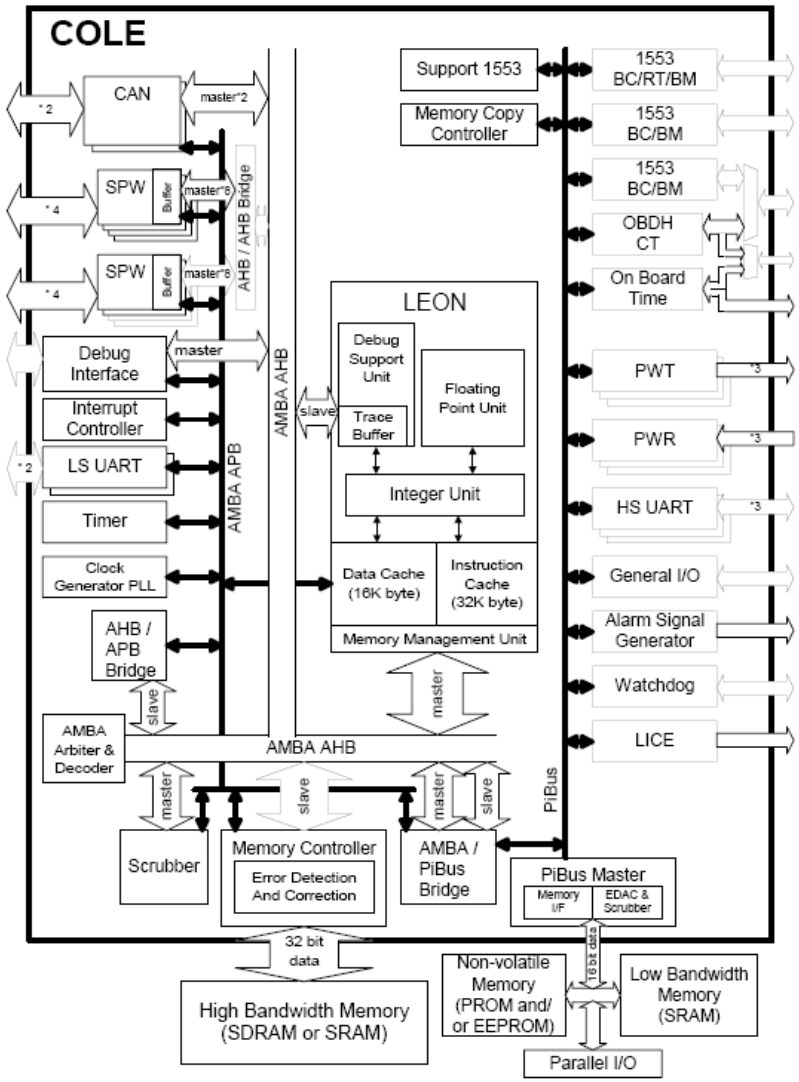
TM Telemetry - Sources

- Sources of Telemetry allocated to separate VC Virtual Channels
  - Hardware generated TM's:
    - Emergency telemetry: reporting of essential Telemetry: SW independent – low bandwidth <0,2 Kbps
    - Context memory (REM) dumps - < 6Kbps
  - Processor generated TM
    - Event driven TM's, housekeeping, off-line and Mass Memory data… See SW design
  - TM from other sources (payloads, instruments) that inject directly TM without OBSW intervention
  - Idle packet generation: to keep the space link operational and synchronised if no real TM is available
- VCM (Virtual Channels Multiplexer):
  - Time multiplexes VC's according to BAT (Bandwidth Allocation Table) on a per frame basis

Telemetry Encoder

- Handles the serialised TM frames:
  - Addition of Reed-Solomon Error Detection and Correction symbols
  - Pseudo-randomisation (to ensure bit transition density and avoid Tx DC components)
  - Optional Non-Return-to-Zero Mark encoding
  - Convolutional Encoding, such as Viterbi (doubles the bit rate)
  - Optional Split-Phase Level modulator (doubles bit rate)
  - Feed bitstream to radio amplifier/transmitter

OBC: System on Chip



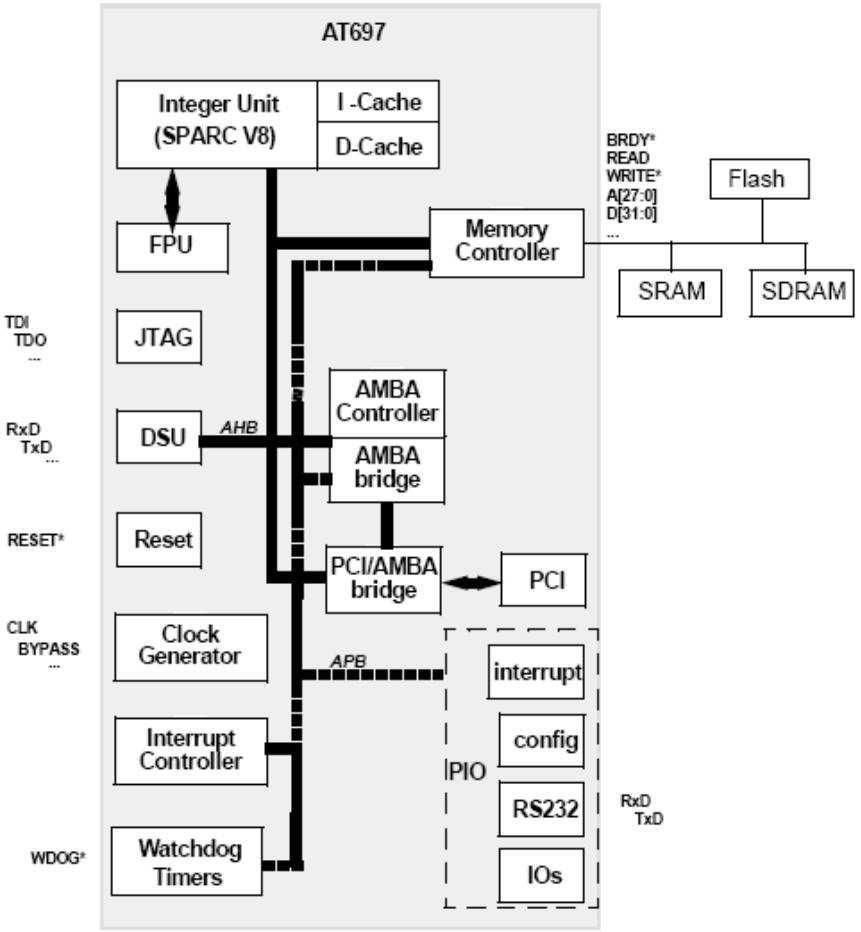
- Saab Space, available in 2008 in Atmel ATC18RHA radiation hard 180 nm standard cell ASIC technology
- LEON2-FT Fault Tolerant SPARC V8 processor, 86 MIPS@100 MHz + FPU
- SPARC V8 Reference Memory Management Unit (MMU)
- Caches: 32 KB instruction, 16 KB data cache
- Extended Debug Support Unit (E-DSU) with 4096 trace lines
- EDAC and automatic scrubbing on large SDRAM, Memory Copy Controller
- 3 High-Speed UART's
- Three MIL-STD-1553B bus interfaces
- OBDH bus Central Terminal
- 3 PacketWire Receivers & Transmitters
- 8 ECSS-E-50-12A SpaceWire Interfaces capable up to 200 MHz/160 Mbps, Hardware support for Remote Memory Access Protocol.
- 2 Controller Area Network (CAN) interfaces supporting up to 1 Mbps

Reconfiguration Module

- Manages:
  - The watchdog and associated computer reset and switch-over logic
  - The active and cold standby computer
  - The OBSW version to be loaded at start-up
- It can as well contain:
  - Context memory:
    - Serves as memory for time stamped logs of reconfiguration module, boot and application SW
    - Is not reset by a computer boot and regularly transferred to the ground.
  - Emergency TC hardware decoder and pulse generator
  - Central date and time system

OBP EXAMPLES

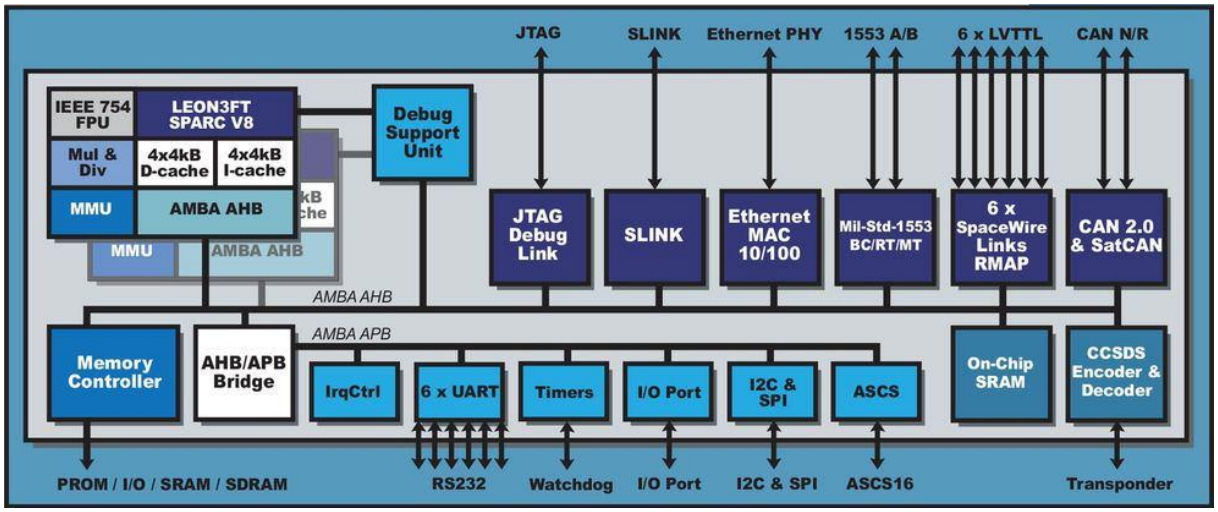
OBP : LEON2



- Synthesisable Open Source VHDL model of a 32-bit SPARC V8
- Caches: 16 KB Data, 32 KB instructions
- Self standing computer: need only external clock and memory
- 2 timers + watchdog
- 2 UART, 32 parallel I/O
- Fault tolerant (parity, EDAC, TMR)
- Separate DSU (Debug Serial Unit) with normal serial line interface and transaction/instruction trace buffer with 512 entries
- Integrated PCI interface (50 % of chip)
- Virtual latchup free (70 MeV.cm^2/mg)
- Radiation up to 300 Krads (Si)

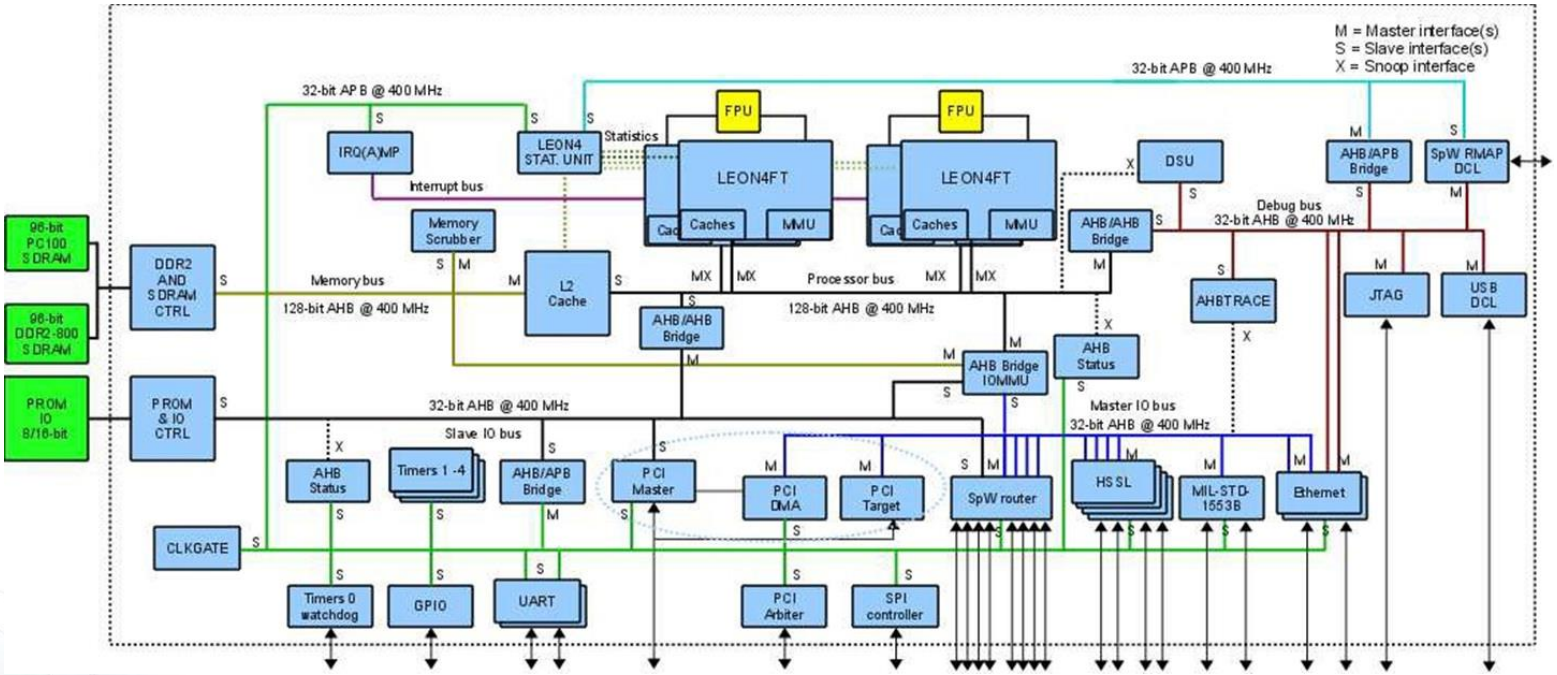
SPARC = Scalable Processor ARChitecture = RISC (Reduced Instruction Set Computer) – 32 bit
RISC = Simple instruction set, simple CPU, target = 1 instruction per cycle (without memory R/W)
simple compiler, but needs 40 % bigger code size, better code optimisation
SUN SPARC strong points: One of the best performance & power figures per gate
SPARC architecture is no longer evolving but still holds up against other CPU designs

OBP: Dual Core LEON3



GR712RC Architecture © Aeroflex Gaisler AB

OBP: Quad Core LEON4

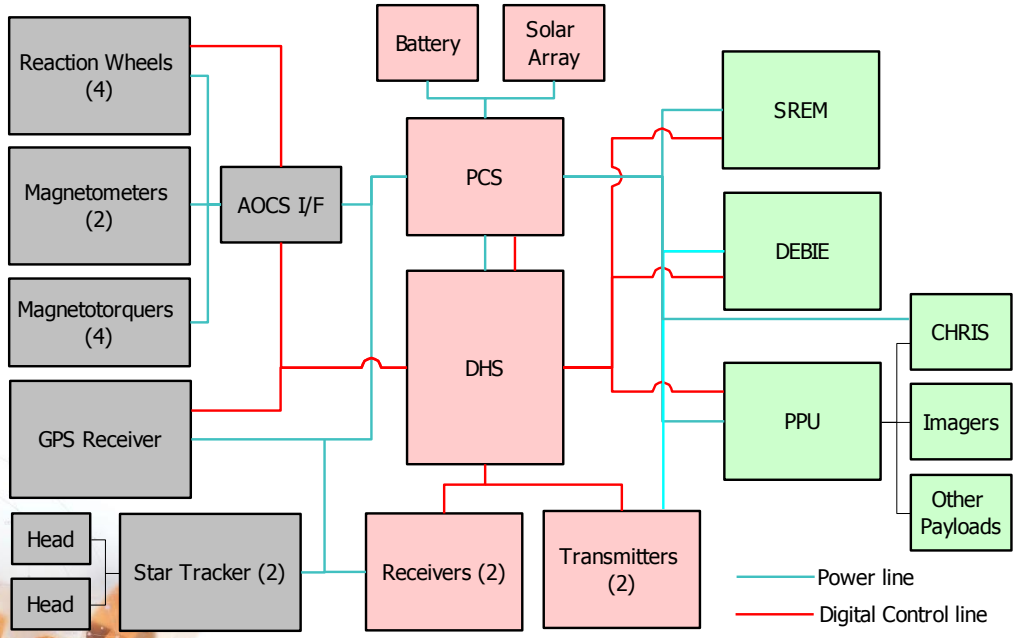


NGMP Architecture © Aeroflex Gaisler AB

AVIONICS EXAMPLES

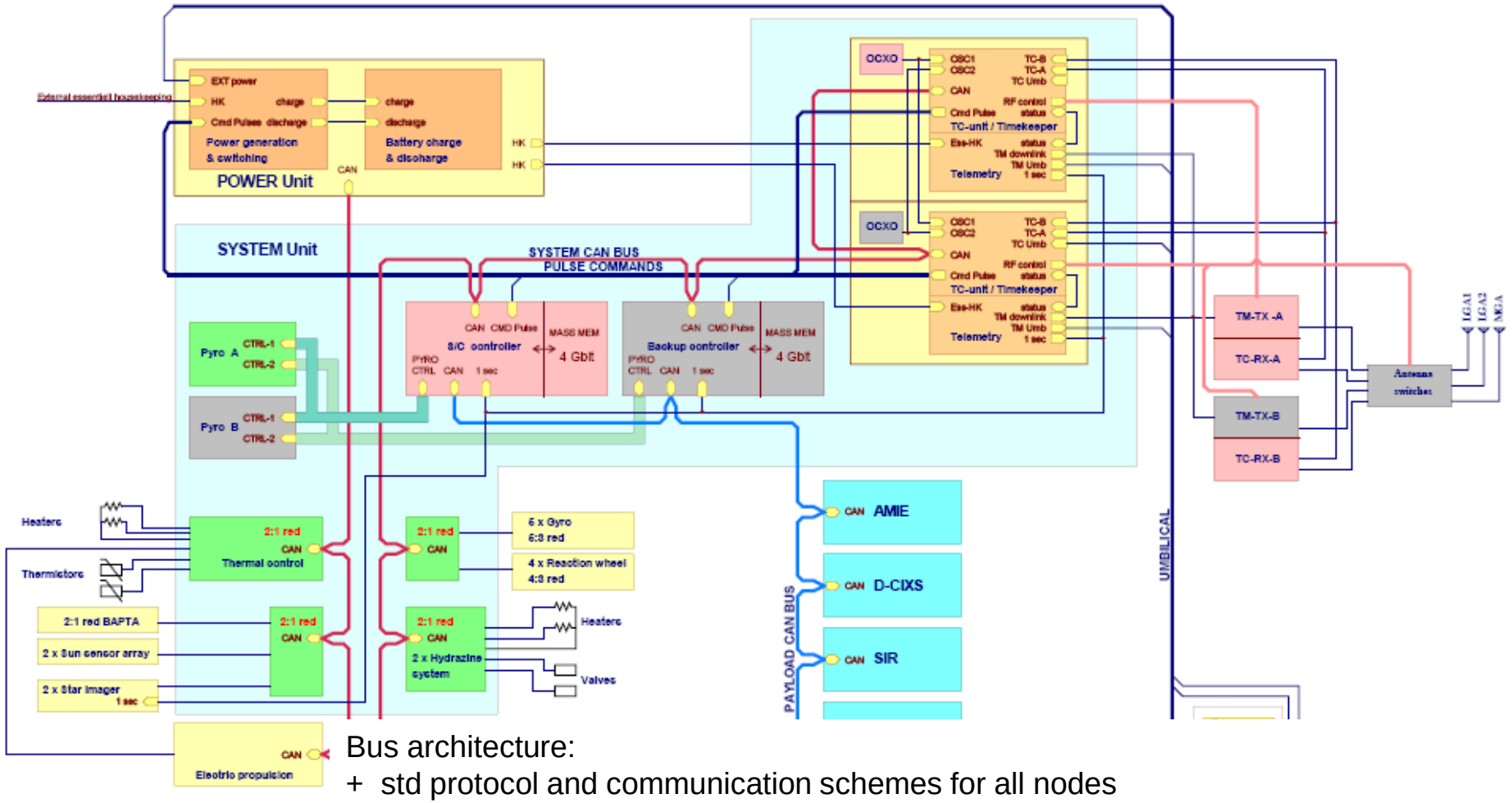
PROBA 1

Proba 1
•Centralized (star) architecture
+ Simple design, direct connection with the OBC
+ Well adapted to off the shelf equipment integration
- Modularity
- Harness



- **Mass:**
  - **Structure** 29kg
  - **Instruments** 24kg
  - **Power** 12kg
  - **AOCS** 9.5kg
  - **Avionic & data processing** 8.5kg
  - **RF** 6kg
  - **Harness** 8kg

SMART-1 Avionics architecture ver 4.2

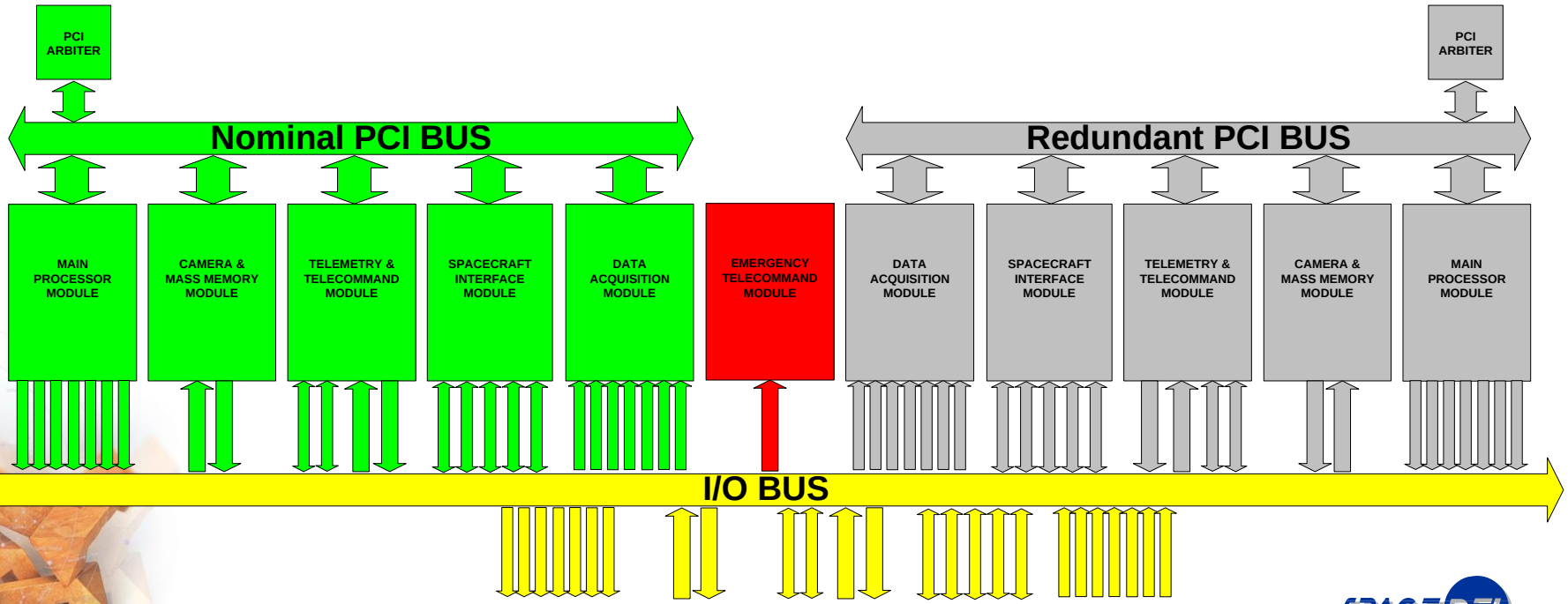


Bus architecture:

+ std protocol and communication schemes for all nodes
+ modularity/ testablity
+ Bus traffic solved with central arbitration (CAN, 1553) or protocal arbitration (CAN, Ethernet)
-I/F component must be developped
- Bus redundancy

PROBA 2 Architecture

•Proba 2
• Internal busses (industrial standards)
• Main Boards/ generic communication (analog/ digital I/Os, serial lines)



Proba2: Main Facts & Figures

Processor board
- 100MIPS
- 64 Mbyte SDRAM
- 4 Mbyte SRAM
- 4 Mbyte Flash
- 256 kByte Prom

Budgets:
Mass 13 kg
Volume 455x160x26[illegible]
Power 17 W

1 failure tolerant system

Power distribution
- 24 outputs of 28V / 50W
- current protected with auto restart
- switchable or non-switchable
- battery undervoltage protected with auto switch off

Telecommand
- 2 Mbps uplink capability
- 4 virtual channels or more
- configurable N° of MAP-ID
- 56 CPDU channels

Centralised time synchronisation

Power conditioning
- Up to 300W satellite peak power
- Up to 6 solar sections

Mass memory
- 4 Gbit
- with EDAC

Context memory
- 128 kbyte
- with EDAC

Telemetry
- 100 Mbps downlink
- 5 virtual channels
- 2 packetwire inputs
- full encoding

Time interfaces
- 8 programmable clock outputs
- 3 clock datation inputs

H/W recovery TC decoder

Communication Interfaces
- Up to 25 UART channels
- Up to 6 TTC-B-01 channels
- a camera interface with frame grabber
- 2 packetwires

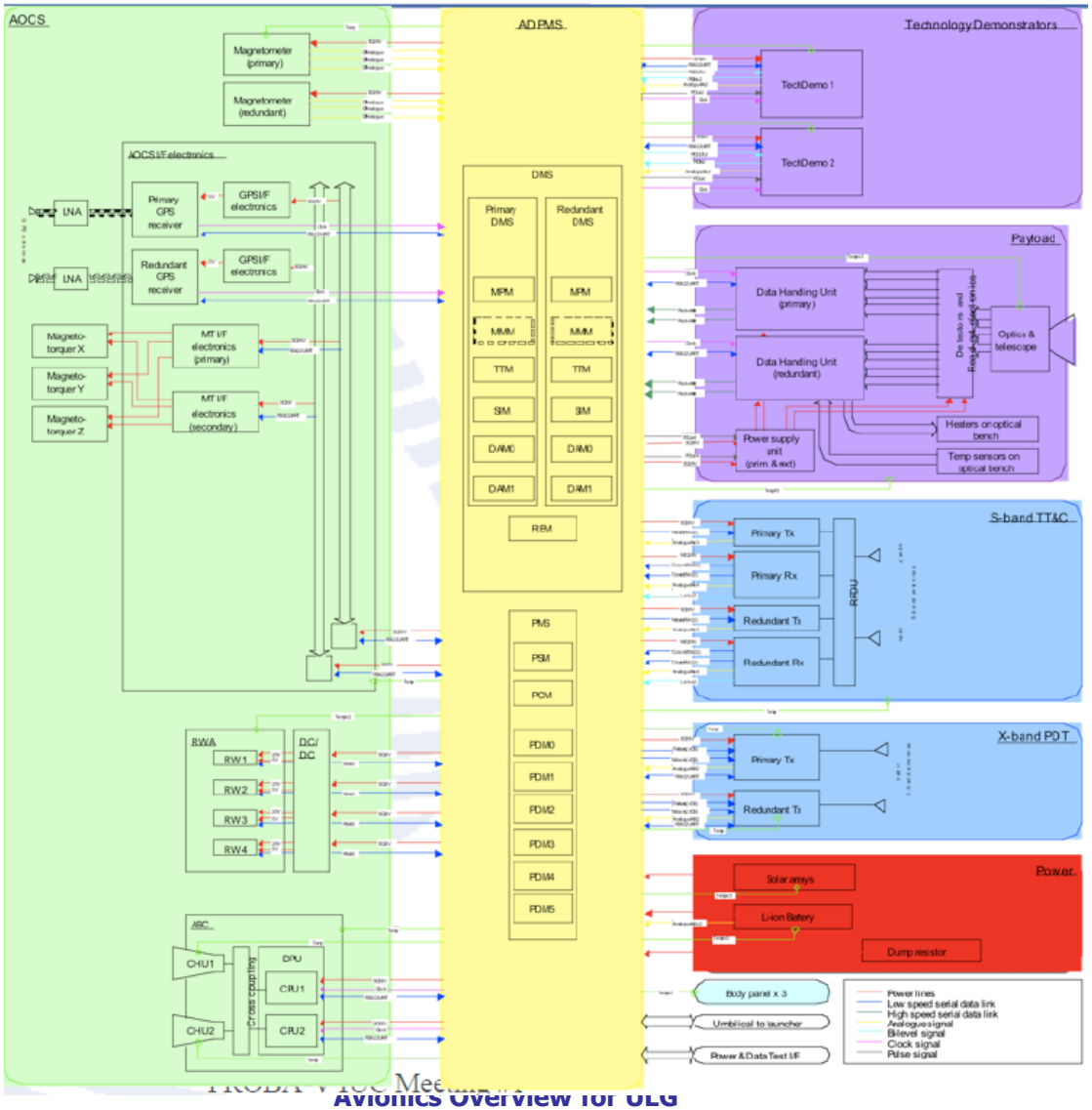
H/W generated emergency telemetry

Analogue Interfaces
- Up to 80 analogue inputs
- Up to 32 temperature inputs

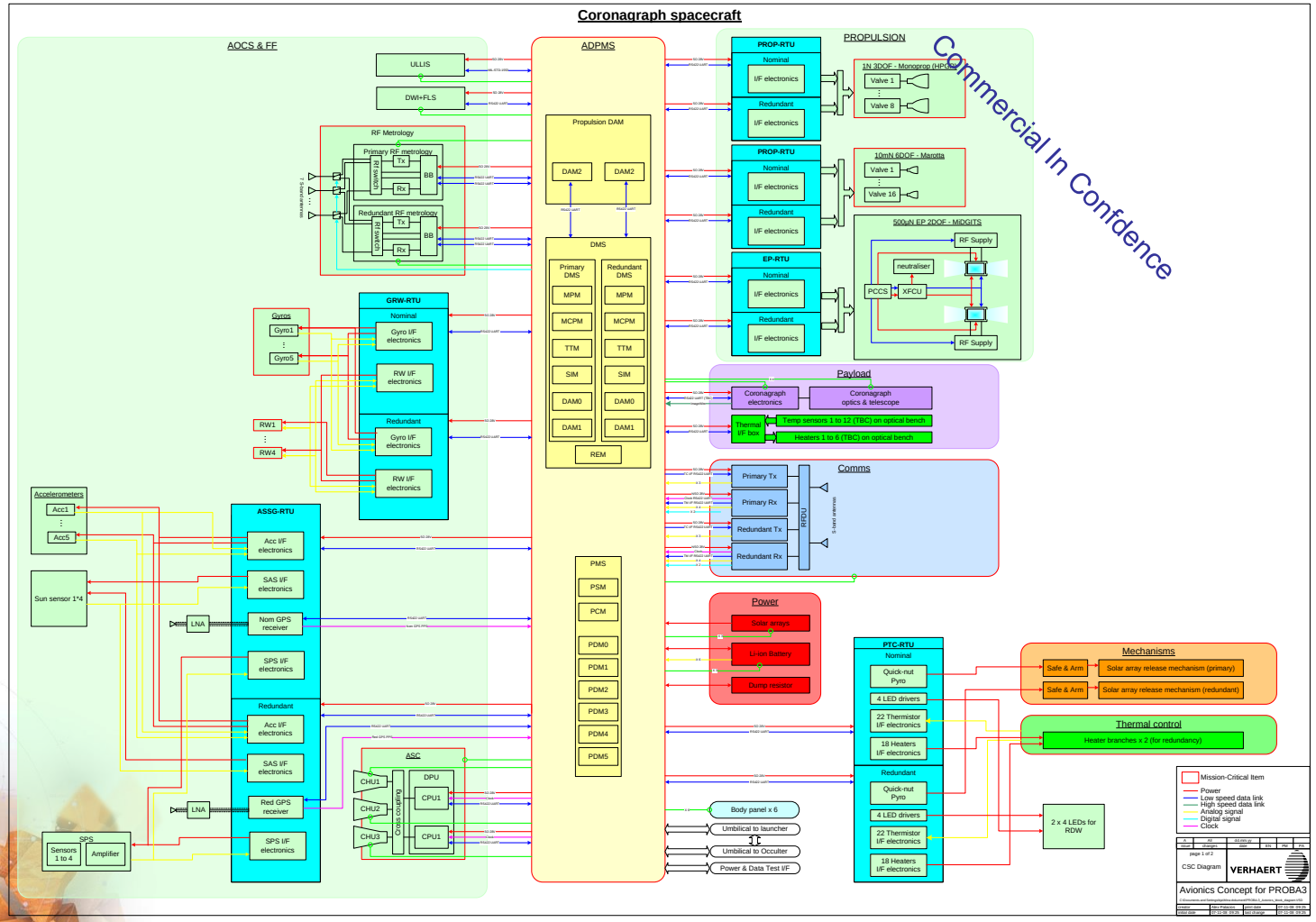
Multi processor support

Backplane data throughput up to 1 GBps

Avionics : Proba V

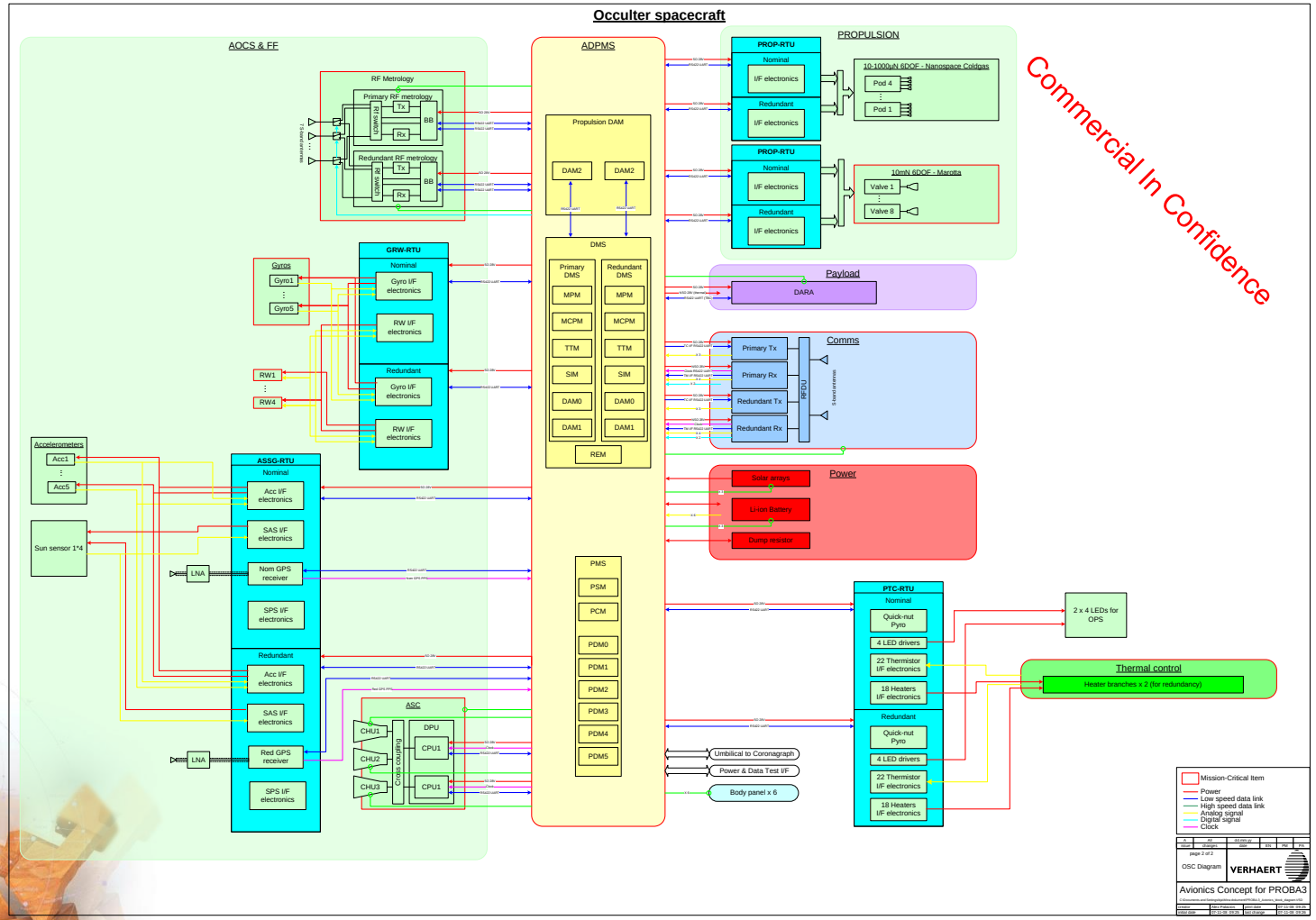


Avionics : Proba 3



Courtesy QinetiQ Space

PROBA 3:



Courtesy QinetiQ Space